UNITED STATES PATENT AND TRADEMARK OFFICE

een

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,563	06/19/2003	Lawrence C. Gunn III	LUX-P003	6066

7590 09/27/2007

Fernandez & Associates, LLP
PO Box D
Menlo Park, CA 94026-6402

EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

MAIL DATE	DELIVERY MODE
09/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

Office Action Summary	Application No.	Applicant(s)
	10/600,563	GUNN ET AL.
	Examiner	Art Unit
	Thomas L. Dickey	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on 13 February 2007.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1,2,5-61 and 63-73 is/are pending in the application.

4a) Of the above claim(s) 36 and 37 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,2,5-61 and 63-73 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 02/13/2007 has been entered.

Priority

2. Acknowledgement is made of applicant's claim for domestic priority under 35 U.S.C. 119(e), through one or more of the provisional applications 60/389962, filed 6/19/02; 60/391277, filed 6/24/02; 60/432925, filed 12/12/02; and 60/433470, filed 12/13/02.

Applicant should note, however, that the written description of one of the above referenced provisional applications must adequately support the subject matter of one of the claims of the instant application in order for that particular claim to be entitled, under 119(e), to the filing date of that particular provisional application. See 35 U.S.C. 119(e); *New Railhead Mfg., L.L.C. v. Vermeer Mfg. Co.*, 298 F.3d 1290, 1294, 63 USPQ2d 1843, 1846 (Fed. Cir. 2002), ("the specification of the provisional must 'contain a written description of the invention and the manner and process of making and using it, in such full, clear, concise, and exact terms,' 35 U.S.C. § 112 ¶1, to enable an ordinarily skilled artisan to practice the invention claimed in the nonprovisional application"); and MPEP § 201.11 ("If a claim in the nonprovisional application is not adequately supported by the written description and drawing(s) (if any) of the provisional application (as in *New Railhead*), that claim in the nonprovisional application is not entitled to the benefit of the filing date of the provisional application"). Note that "adequate support" means that the

disclosure in the provisional application must describe the present claim combination in the "full, clear, concise, and exact terms" required by 35 U.S.C. § 112 ¶1.

Applicant should further note that when the present claim is to a combination, the prior disclosure must describe the combination <u>as a combination</u> (not merely its distinct constituent parts) to meet the requirements of 35 U.S.C. § 112 ¶1. See *Hyatt v. Dudas*, 83 USPQ2d 1373, 1374 (Fed. Cir. 2007)

Information Disclosure Statement

3. If applicant is aware of any relevant prior art, he/she requested to cite it on form **PTO-1449** in accordance with the guidelines set forth in M.P.E.P. 609. It is noted that on 1/24/05 Applicants stated, "The current invention is a waveguide photodetector coupled to a conventional transistor." It would very useful to have on record the prior art sources from which Applicants learned the art of the "conventional transistor."

Claim Objections

4. Applicants list claim 3 as "WITHDRAWN" despite the fact that claim 3 was cancelled on 5/30/06. This is improper.

Applicants list claims 1,2, and 11 "WITHDRAWN" despite the fact that these claims are not subject to restriction. This is improper.

Claim 42 includes two separate sentences, one ending with the words, a plurality of dielectric materials," on page 15, the next ending with the words, "a second plurality of conductive contacts coupled to the silicon," on page 16. This is improper.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

Claims 39-41 and 70 are rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter.

Federal courts have held that 35 U.S.C. § 101 does have certain limits. First, the phrase "anything under the sun that is made by man" is limited by the text of 35 U.S.C. § 101, meaning that one may only patent something that is a machine, manufacture, composition of matter or a process. See, e.g., *In re Alappat*, 33 F.3d 1526, 1542, 31 USPQ2d 1545, 1556 (Fed. Cir. 1994) (in banc); *In re Warmerdam*, 33 F.3d 1354, 1358, 31 USPQ2d 1754, 1757 (Fed. Cir. 1994).

Descriptive material can be characterized as either "functional descriptive material" or "nonfunctional descriptive material." In this context, "functional descriptive material" consists of data structures and computer programs that impart functionality when employed as a computer component. (The definition of "data structure" is "a physical or logical relationship among data elements, designed to support specific data manipulation functions." The New IEEE Standard Dictionary of Electrical and Electronics Terms

308 (5th ed. 1993).) "Nonfunctional descriptive material" includes but is not limited to music, literary works and a compilation or mere arrangement of data.

Both types of "descriptive material" are nonstatutory when claimed as descriptive material per se. *In re Warmerdam*, 33 F.3d at 1360, 31 USPQ2d at 1759. When functional descriptive material is recorded on some computer-readable medium it becomes structurally and functionally interrelated to the medium and will be statutory in most cases since use of technology permits the function of the descriptive material to be realized. Compare examples found in *In re Lowry*, 32 F.3d 1579, 1583-84, 32 USPQ2d 1031, 1035 (Fed. Cir. 1994) (claim to data structure stored on a computer readable medium that increases computer efficiency held statutory) and *Warmerdam*, 33 F.3d at 1360-61, 31 USPQ2d at 1759 (claim to computer having a specific data structure stored in memory held statutory product-by-process claim) with example found in *Warmerdam* at 1361 (31 USPQ2d at 1760) (claim to a data structure per se held nonstatutory). Note that descriptive material can include a description of a functional device and still qualify as nonfunctional descriptive material.

Applicants' claims 39-41 and 70 are drawn to a "data structure representation" of a physical device. Such a representation, if recorded on some computer-readable medium, does not become structurally and functionally interrelated to the medium except for the limited purpose of storing a description of the physical device being represented. As such these claims are drawn to subject matter that is per se nonstatutory. *Warmer-*

dam, 33 F.3d at 1361; 31 USPQ2d at 1760. See also "Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility," United States Patent and Trademark Office OG Notices: 22 November 2005 (available at http://www.uspto.gov/web/offices/com/sol/og/2005/week47/patgupa.htm).

Applicants' attention is drawn to the fact that a "data structure representation" of Applicants' disclosed device is already stored on this Office's computers, along with millions of other "data structure representation" of other disclosed devices, compositions of matter, and processes. Does Applicant believe that the patent laws require this Office to allow claims (should the millions of inventors of these millions of applications submit claims to "data structure representations" of their inventions) that this Office would infringe by simply performing the duties prescribed by said patent laws?

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

A. Claims 42 and 43 recite a "plurality of mask works comprising a pattern of opaque and transparent areas adapted to define a germanium on silicon waveguide photodetector [a physical device]. It is understood that the description of the physical device defines the plurality of mask works but the physical device is not itself required to be present in the claimed plurality of mask works. The recitation of the "germanium on silicon waveguide photodetector" is rather intended to define the precise limits of the mask works being claimed.

A mask work is

> a series of related images, however fixed or encoded—
>
> (A) having or representing the predetermined, three-dimensional pattern of metallic, insulating, or semiconductor material present or removed from the layers of a semiconductor chip product; and
>
> (B) in which series the relation of the images to one another is that each image has the pattern of the surface of one form of the semiconductor chip product;

17 United States Code § 901. Mask works are thus defined as original works fixed in tangible media. As such they are copyrightable under 17 USC § 905. Also as such, they come under scrutiny for conformance with the so-called "printed matter doctrine."

Printed matter (including graphics "adapted to define a germanium on silicon waveguide photodetector") incorporated into an underlying object serves to help define patentable subject matter if the printed matter is functionally related to the underlying object. *In re Gulack*, 703 F.2d 1381, 1387, 217 USPQ 401, 408 (Fed. Cir. 1983). However, a requirement that the underlying object include words or graphics to "define" other subject matter (whether the other subject matter be patentable or not) is not <u>functionally</u> related to the underlying object. See *In re Ngai,* 367 F3d 1336, 1337, 70

USPQ2d 1862, 1864 (Fed. Cir. 2004). Use of the underlying object to define other subject matter amounts to nothing more than a new use for the underlying object. Id.

Claims 42 and 43 are therefore rejected under 35 U.S.C. 102(b) as anticipated by ROTTMANN (3,442,583).

Rottmann discloses a plurality of mask works comprising a pattern of opaque and transparent areas adapted to define a semiconductor device. Claims 42 and 43 require Rottmann's mask work to be "adapted to define a [particular] germanium on silicon waveguide photodetector," but the words "adapted to" clearly show applicants merely intend to define a new use for Rottmann's old device. Again, see *In re Ngai,* 367 F3d at 1337, 70 USPQ2d at 1864.

B. Claims 1,2,5-38,42-61, 63-69,and 71-73 are rejected under 35 U.S.C. § 102(e) as being anticipated by KNIGHTS ET AL. (2006/0039666).

With regard to claims 1,2, and 11 Knights et al. discloses a waveguide photodetector comprising a waveguide 50 comprising a core 70 comprised of a germanium 71,72 on silicon 70 heterojunction stack comprising a silicon layer 70 comprising substantially silicon for conducting light, a germanium layer 71,72 comprising substantially germanium for conducting light; and a cladding 106,109 (13,15 in figure 1) comprised of a plurality of SiO_2 dielectric materials, a first plurality of conductive contacts 63a (compare figure 10 of Knights et al. to figure 2 of the instant application) coupled to said germanium layer 71,72, and a second plurality of conductive contacts 63b coupled to said sili-

con layer 70, wherein the germanium 71,72 on silicon 70 heterojunction forms a diode structure with a depletion region, where the diode structure is capable of producing and separating electron hole pairs caused by photons absorbed in the depletion region, further comprising the fabrication of a transistor body at the same time as the fabrication of the silicon of the heterojunction. Note figures 1-4, 8-13, 15, 16, 18, and paragraphs 0031-0106 and 0114-0125 of Knights et al.

With regard to claims 5-10 Knights et al. discloses a waveguide photodetector comprising a waveguide 50 comprising a core 70 comprised of a germanium 71,72 on silicon 70 heterojunction stack comprising a silicon layer 70 comprising substantially silicon for conducting light, a germanium layer 71,72 comprising substantially germanium for conducting light; and a cladding 106,109 (13,15 in figure 1) comprised of a plurality of dielectric materials, a first plurality of conductive contacts 63a (compare figure 10 of Knights et al. to figure 2 of the instant application) coupled to said germanium layer 71,72, and a second plurality of conductive contacts 63b coupled to said silicon layer 70, wherein the germanium 71,72 on silicon 70 heterojunction forms a diode structure with a depletion region, where the diode structure is capable of producing and separating electron hole pairs caused by photons absorbed in the depletion region, wherein the cladding 106,109 further comprises a bottom cladding 106 comprised of the insulating layer of an SOI (SEE PARAGRAPH 0012) that also serves as the substrate of a CMOS integrated circuit (not shown, see paragraph 0031), a top and side cladding 109 where

each of the claddings is comprised of a plurality of dielectric materials, one of the plurality of dielectric materials comprising the top and side cladding 109 are formed from the same film as an inter-layer dielectric film, gate spacer, dielectric spacer, passivation film, isolation dielectric or field oxide of a floating body or body tied CMOS transistor. Note figures 1-4, 8-13, 15, 16, 18, and paragraphs 0031-0106 and 0114-0125 of Knights et al.

With regard to claims 12-19 Knights et al. discloses a waveguide photodetector comprising a waveguide 50 comprising a core 70 comprised of a germanium 71,72 on silicon 70 heterojunction stack comprising a silicon layer 70 comprising substantially silicon for conducting light, a germanium layer 71,72 comprising substantially germanium for conducting light; and a cladding 106,109 (13,15 in figure 1) comprised of a plurality of dielectric materials, a first plurality of conductive contacts 63a (compare figure 10 of Knights et al. to figure 2 of the instant application) coupled to said germanium layer 71,72, and a second plurality of conductive contacts 63b coupled to said silicon layer 70, wherein the germanium 71,72 on silicon 70 heterojunction forms a diode structure with a depletion region, where the diode structure is capable of producing and separating electron hole pairs caused by photons absorbed in the depletion region, wherein each of the second plurality of conductive contacts 63b comprises a metal silicide ohmic contact to the silicon layer 70 of the heterojunction, and a tungsten conductive plug 19,20 with a first terminal (i.e., first end of plug 19,20) coupled to the ohmic

contact and a second terminal (i.e., second end of the plug) coupled to a metal layer of an integrated circuit (not shown, see paragraph 0031) and the conductive plug 19,20 is formed simultaneously with the metal layer, further comprising the fabrication of an ohmic contact on the source, drain, body, or gate of a transistor at the same time as the fabrication of an ohmic contact on the silicon of the heterojunction; the fabrication of a conductive plug 19,20 to an ohmic contact of a transistor at the same time as the fabrication of the conductive plug 19,20 to an ohmic contact to the silicon of the heterojunction, and the fabrication of a tungsten or aluminum local interconnection between a pair of transistors, at the same time as fabricating a local interconnection for coupling an ohmic contact on the silicon of the heterojunction with an ohmic contact on one of the transistors. Note figures 1-4, 8-13, 15, 16, 18, and paragraphs 0031-0106 and 0114-0125 of Knights et al.

With regard to claim 20 Knights et al. discloses a waveguide photodetector comprising a waveguide 50 comprising a core 70 comprised of a germanium 71,72 on silicon 70 heterojunction stack comprising a silicon layer 70 comprising substantially silicon for conducting light, a germanium layer 71,72 comprising substantially germanium for conducting light; and a cladding 106,109 (13,15 in figure 1) comprised of a plurality of dielectric materials, a first plurality of conductive contacts 63a (compare figure 10 of Knights et al. to figure 2 of the instant application) coupled to said germanium layer 71,72, and a second plurality of conductive contacts 63b coupled to said silicon layer

70, wherein the germanium 71,72 on silicon 70 heterojunction forms a diode structure with a depletion region, where the diode structure is capable of producing and separating electron hole pairs caused by photons absorbed in the depletion region, wherein at least one contact of the pluralities of contacts is coupled to a metal layer on an integrated circuit (not shown, see paragraph 0031), where the metal layer has a coupling to a resistor, inductor, capacitor, diode, bond pad, or transistor on the integrated circuit (not shown, see paragraph 0031). Note figures 1-4, 8-13, 15, 16, 18, and paragraphs 0031-0106 and 0114-0125 of Knights et al.

With regard to claim 21 Knights et al. discloses a waveguide photodetector comprising a waveguide 50 comprising a core 70 comprised of a germanium 71,72 on silicon 70 heterojunction stack comprising a silicon layer 70 comprising substantially silicon for conducting light, a germanium layer 71,72 comprising substantially germanium for conducting light; and a cladding 106,109 (13,15 in figure 1) comprised of a plurality of dielectric materials, a first plurality of conductive contacts 63a (compare figure 10 of Knights et al. to figure 2 of the instant application) coupled to said germanium layer 71,72, and a second plurality of conductive contacts 63b coupled to said silicon layer 70, wherein the germanium 71,72 on silicon 70 heterojunction forms a diode structure with a depletion region, where the diode structure is capable of producing and separating electron hole pairs caused by photons absorbed in the depletion region, wherein each of the first plurality of conductive contacts 63a comprises an ohmic contact to the

germanium of the heterojunction, and a conductive plug 19,20 with a first terminal (i.e., first end of plug 19,20) coupled to the ohmic contact and a second terminal (i.e., second end of the plug) coupled to a metal layer of an integrated circuit (not shown, see paragraph 0031). Note figures 1-4, 8-13, 15, 16, 18, and paragraphs 0031-0106 and 0114-0125 of Knights et al.

With regard to claims 22-27 Knights et al. discloses a waveguide photodetector comprising a waveguide 50 comprising a core 70 comprised of a germanium 71,72 on silicon 70 heterojunction stack comprising a silicon layer 70 comprising substantially silicon for conducting light, a germanium layer 71,72 comprising substantially germanium for conducting light; and a cladding 106,109 (13,15 in figure 1) comprised of a plurality of dielectric materials, a first plurality of conductive contacts 63a (compare figure 10 of Knights et al. to figure 2 of the instant application) coupled to said germanium layer 71,72, and a second plurality of conductive contacts 63b coupled to said silicon layer 70, wherein the germanium 71,72 on silicon 70 heterojunction forms a diode structure with a depletion region, where the diode structure is capable of producing and separating electron hole pairs caused by photons absorbed in the depletion region, further comprising the introduction of a first plurality of dopants into a plurality of regions in the silicon layer 70 of the heterojunction and the silicon body of a transistor, and the introduction of a second plurality of dopants into a plurality of regions in the germanium layer 71,72 of the heterojunction, wherein the first plurality of dopants is comprised of

dopants with electrical charge opposite or equal to the polarity of the dopants comprising the second plurality of dopants. Note figures 1-4, 8-13, 15, 16, 18, and paragraphs 0031-0106 and 0114-0125 of Knights et al.

With regard to claims 28-33 Knights et al. discloses a waveguide photodetector comprising a waveguide 50 comprising a core 70 comprised of a germanium 71,72 on silicon 70 heterojunction stack comprising a silicon layer 70 comprising substantially silicon for conducting light, a germanium layer 71,72 comprising substantially germanium for conducting light; and a cladding 106,109 (13,15 in figure 1) comprised of a plurality of dielectric materials, a first plurality of conductive contacts 63a (compare figure 10 of Knights et al. to figure 2 of the instant application) coupled to said germanium layer 71,72, and a second plurality of conductive contacts 63b coupled to said silicon layer 70, wherein the germanium 71,72 on silicon 70 heterojunction forms a diode structure with a depletion region, where the diode structure is capable of producing and separating electron hole pairs caused by photons absorbed in the depletion region, further comprising a silicon waveguide 50 with an input and an output; and, a transistor with polysilicon gate; a polysilicon optical structure mode converter 122 with an input and an output, where the output of the mode converter 122 is coupled to the input of the waveguide photodetector, and the input to the mode converter 122 is coupled to the output of the silicon waveguide 50, wherein the mode converter 122 is comprised of a plurality of dielectric structures introduced in substantial proximity to the input to the

waveguide photodetector. Note figures 1-4, 8-13, 15, 16, 18, and paragraphs 0031-0106 and 0114-0125 of Knights et al.

With regard to claim 38 A semiconductor chip comprising a germanium on silicon waveguide photodetector located on the semiconductor chip, said germanium on silicon waveguide photodetector comprising a waveguide 50 comprising a core 70 comprised of a germanium 71,72 on silicon 70 heterojunction stack comprising a silicon layer 70 comprising substantially silicon for conducting light, and a germanium layer 71,72 comprising substantially germanium for conducting light; and a cladding 106,109 (13,15 in figure 1) comprised of a plurality of dielectric materials; an optical input; a first plurality of conductive contacts 63a (compare figure 10 of Knights et al. to figure 2 of the instant application) coupled to said germanium layer 71,72; and a second plurality of conductive contacts 63b coupled to said silicon layer 70; and, inputs for receiving optical signals; outputs for outputting electrical signals; and, a semiconductor device (not shown, see paragraph 0031) connected to the germanium on silicon waveguide photodetector outputs and located on the semiconductor chip. Note figures 1-4, 8-13, 15, 16, 18, and paragraphs 0031-0106 and 0114-0125 of Knights et al.

With regard to claim 44 Knights et al. discloses a waveguide photodetector comprising a waveguide 50 comprising a core 70 comprised of a germanium 71,72 on silicon 70 heterojunction, and cladding 106,109 comprised of a plurality of dielectric materials, a first plurality of conductive contacts 63a (compare figure 10 of Knights et al. to figure 2

of the instant application) coupled to the germanium 71,72 and not coupled to the silicon 70; a second plurality of electrical contacts 63b coupled to the silicon 70 and not coupled to the germanium 71,72, and wherein said first plurality of conductive contacts 63a are displaced from said second plurality of conductive contacts 63b; and, a transistor body fabricated at the same time as the fabrication of the silicon of the heterojunction. Note figures 1-4, 8-13, 15, 16, 18, and paragraphs 0031-0106 and 0114-0125 of Knights et al.

With regard to claim 45 Knights et al. discloses a waveguide photodetector comprising a waveguide 50 comprising a core 70 comprised of a germanium 71,72 on silicon 70 heterojunction wherein the germanium 71,72 on silicon 70 heterojunction forms a diode structure with a depletion region, where the diode structure is capable of producing and separating electron hole pairs caused by photons absorbed in the depletion region, and a cladding 106,109 (13,15 in figure 1) comprised of a plurality of dielectric materials; and, a first plurality of conductive contacts 63a (compare figure 10 of Knights et al. to figure 2 of the instant application) coupled to the germanium 71,72; and, a second plurality of electrical contacts 63b coupled to the silicon 70. Note figures 1-4, 8-13, 15, 16, 18, and paragraphs 0031-0106 and 0114-0125 of Knights et al.

With regard to claims 46-50 Knights et al. discloses a waveguide photodetector comprising a waveguide 50 comprising a core 70 comprised of a germanium 71,72 on silicon 70 heterojunction, a cladding 106,109 (13,15 in figure 1) comprised of a plurality

of dielectric materials; a first plurality of conductive contacts 63a (compare figure 10 of Knights et al. to figure 2 of the instant application) coupled to the germanium 71,72, and a second plurality of electrical contacts 63b coupled to the silicon 70; wherein the cladding 106,109 comprises a bottom cladding 106 comprised of the insulating layer of an SOI (SEE PARAGRAPH 0012) that also serves as the substrate of a CMOS integrated circuit (not shown, see paragraph 0031), a top and side cladding 109 each of the claddings is comprised of a plurality of dielectric materials, and one of the plurality of dielectric materials comprising the top and side cladding 109 is formed from the same film as a dielectric component of a transistor, where the dielectric component is selected from a group comprising an inter-layer dielectric film, a gate spacer, a silicide block, a dielectric spacer, a passivation film, an isolation dielectric and a field oxide. Note figures 1-4, 8-13, 15, 16, 18, and paragraphs 0031-0106 and 0114-0125 of Knights et al.

With regard to claims 51-58 Knights et al. discloses a waveguide photodetector comprising a waveguide 50 comprising a core 70 comprised of a germanium 71,72 on silicon 70 heterojunction, and a cladding 106,109 (13,15 in figure 1) comprised of a plurality of dielectric materials, a first plurality of conductive contacts 63a (compare figure 10 of Knights et al. to figure 2 of the instant application) coupled to the germanium 71,72, and a second plurality of electrical contacts 63b coupled to the silicon 70 wherein each of the second plurality of conductive contacts 63b comprises a metal silicide ohmic contact to the silicon of the heterojunction, and a tungsten conductive plug 19,20 with a

first terminal (i.e., first end of plug 19,20) coupled to the ohmic contact and a second terminal (i.e., second end of the plug) coupled to a metal layer of an integrated circuit (not shown, see paragraph 0031), wherein the conductive plug 19,20 is formed simultaneously with the metal layer, and further comprising the fabrication of an ohmic contact on the source, drain, body, or gate of a transistor at the same time as the fabrication of an ohmic contact on the silicon of the heterojunction, the fabrication of a conductive plug 19,20 to an ohmic contact of a transistor at the same time as the fabrication of a conductive plug 19,20 to an ohmic contact to the silicon of the heterojunction, and the fabrication of a tungsten or aluminum local interconnection between a pair of transistors, at the same time as fabricating a local interconnection for coupling an ohmic contact on the silicon of the heterojunction with an ohmic contact on one of the transistors. Note figures 1-4, 8-13, 15, 16, 18, and paragraphs 0031-0106 and 0114-0125 of Knights et al.

With regard to claim 59 Knights et al. discloses a waveguide photodetector comprising a waveguide 50 comprising a core 70 comprised of a germanium 71,72 on silicon 70 heterojunction, and a cladding 106,109 (13,15 in figure 1) comprised of a plurality of dielectric materials, a first plurality of conductive contacts 63a (compare figure 10 of Knights et al. to figure 2 of the instant application) coupled to the germanium 71,72 and not coupled to the silicon 70, and, a second plurality of electrical contacts 63b coupled to the silicon 70 and not coupled to the germanium 71,72, wherein said first plurality of

conductive contacts 63a are displaced from said second plurality of conductive contacts 63b; wherein at least one contact of the pluralities of contacts is coupled to a metal layer on an integrated circuit (not shown, see paragraph 0031), where the metal layer has a coupling to a resistor, inductor, capacitor, diode, bond pad, or transistor on the integrated circuit (not shown, see paragraph 0031). Note figures 1-4, 8-13, 15, 16, 18, and paragraphs 0031-0106 and 0114-0125 of Knights et al.

With regard to claim 60 Knights et al. discloses a waveguide photodetector comprising a waveguide 50 comprising a core 70 comprised of a germanium 71,72 on silicon 70 heterojunction, a cladding 106,109 (13,15 in figure 1) comprised of a plurality of dielectric materials, a first plurality of conductive contacts 63a (compare figure 10 of Knights et al. to figure 2 of the instant application) coupled to the germanium 71,72 wherein each of the first plurality of conductive contacts 63a comprises an ohmic contact to the germanium of the heterojunction, and a conductive plug 19,20 with a first terminal (i.e., first end of plug 19,20) coupled to the ohmic contact and a second terminal (i.e., second end of the plug) coupled to a metal layer of an integrated circuit (not shown, see paragraph 0031), and; a second plurality of electrical contacts 63b coupled to the silicon 70. Note figures 1-4, 8-13, 15, 16, 18, and paragraphs 0031-0106 and 0114-0125 of Knights et al.

With regard to claims 61,63, and 64 Knights et al. discloses a waveguide photodetector comprising a waveguide 50 comprising a core 70 comprised of a germa-

nium 71,72 on silicon 70 heterojunction, a cladding 106,109 (13,15 in figure 1) comprised of a plurality of dielectric materials; a first plurality of conductive contacts 63a (compare figure 10 of Knights et al. to figure 2 of the instant application) coupled to the germanium 71,72 and not coupled to the silicon 70; and a second plurality of electrical contacts 63b coupled to the silicon 70 and not coupled to the germanium 71,72, wherein said first plurality of conductive contacts 63a are displaced from said second plurality of conductive contacts 63b, wherein a plurality of regions in the silicon 70 of the heterojunction comprise a first plurality of dopants introduced at the same time as the introduction of a plurality of dopants into a plurality of regions in the silicon body of a transistor(claim 61), a plurality of regions in the germanium 71,72 of the heterojunction comprise a second plurality of dopants, and the first plurality of dopants is comprised of dopants with electrical charge opposite (claim 63) or equal (claim 64) to the polarity of the dopants comprising the second plurality of dopants. Note figures 1-4, 8-13, 15, 16, 18, and paragraphs 0031-0106 and 0114-0125 of Knights et al.

With regard to claims 65-67 Knights et al. discloses a waveguide photodetector having an input and comprising a silicon waveguide 50 with an input and an output and comprising a core 70 comprised of a germanium 71,72 on silicon 70 heterojunction, a cladding 106,109 (13,15 in figure 1) comprised of a plurality of dielectric materials, a first plurality of conductive contacts 63a (compare figure 10 of Knights et al. to figure 2 of the instant application) coupled to the germanium 71,72; a second plurality of electrical con-

tacts 63b coupled to the silicon 70; a transistor having a polysilicon gate; and a polysilicon optical structure mode converter 122 with an input and an output, where the output of the mode converter 122 is coupled to the input of the waveguide photodetector, and where the input to the mode converter 122 is coupled to the output of the silicon waveguide 50 and the mode converter 122 is comprised of a plurality of dielectric structures introduced in substantial proximity to the input to the waveguide photodetector. Note figures 1-4, 8-13, 15, 16, 18, and paragraphs 0031-0106 and 0114-0125 of Knights et al.

With regard to claim 71 Knights et al. discloses a waveguide photodetector comprising a waveguide 50 comprising a core 70 comprised of a germanium 71,72 on silicon 70 heterojunction, and cladding 106,109 comprised of a plurality of dielectric materials, a first plurality of conductive contacts 63a (compare figure 10 of Knights et al. to figure 2 of the instant application) coupled to the germanium 71,72; a second plurality of electrical contacts 63b coupled to the silicon 70; and, a transistor body fabricated at the same time as the fabrication of the silicon of the heterojunction and wherein the transistor body is external to the waveguide 50 and displaced from the waveguide 50. Note figures 1-4, 8-13, 15, 16, 18, and paragraphs 0031-0106 and 0114-0125 of Knights et al.

With regard to claim 72 Knights et al. discloses a waveguide photodetector comprising a waveguide 50 comprising a core 70 comprised of a germanium 71,72 on silicon 70 heterojunction, and a cladding 106,109 (13,15 in figure 1) comprised of a plurality of di-

electric materials, a first plurality of conductive contacts 63a (compare figure 10 of Knights et al. to figure 2 of the instant application) coupled to the germanium 71,72, and a second plurality of electrical contacts 63b coupled to the silicon 70, wherein at least one contact of the pluralities of contacts is electrically coupled to a metal layer on an integrated circuit (not shown, see paragraph 0031), where the metal layer has a an electrical to a resistor, inductor, capacitor, diode, bond pad, or transistor on the integrated circuit (not shown, see paragraph 0031) external to the waveguide 50 and displaced from the waveguide 50. Note figures 1-4, 8-13, 15, 16, 18, and paragraphs 0031-0106 and 0114-0125 of Knights et al.

With regard to claim 73 Knights et al. discloses a waveguide photodetector comprising a waveguide 50 comprising a core 70 comprised of a germanium 71,72 on silicon 70 heterojunction wherein a plurality of regions in the silicon of the heterojunction comprise a plurality of dopants introduced at the same time as the introduction of a plurality of dopants into a plurality of regions in the silicon body of a transistor and wherein the transistor is external to the waveguide 50 and displaced from the waveguide 50, and a cladding 106,109 (13,15 in figure 1) comprised of a plurality of dielectric materials; a first plurality of conductive contacts 63a (compare figure 10 of Knights et al. to figure 2 of the instant application) coupled to the germanium 71,72; and a second plurality of electrical contacts 63b coupled to the silicon 70. Note figures 1-4, 8-13, 15, 16, 18, and paragraphs 0031-0106 and 0114-0125 of Knights et al.

C. Claims 1,2,5-38,42-61, 63-69,and 71-73 are rejected under 35 U.S.C. § 102(b) as being anticipated by DELWALA (2002/0172464).

With regard to claims 1,2, and 11 Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium 108 on silicon 191 heterojunction stack comprising a silicon layer 191 (6301 in figure 55a) comprising substantially silicon for conducting light, a germanium layer 108 (6302 in figure 55a) comprising substantially germanium for conducting light; and a cladding 104-5109 comprised of a plurality of SiO2 dielectric materials, a first plurality of conductive contacts 120 coupled to said germanium layer 108 (6302 in figure 55a), and a second plurality of conductive contacts 118,122 (800 in fig. 43) coupled to said silicon layer 191, wherein the germanium 108 on silicon 191 heterojunction forms a diode structure with a depletion region, where the diode structure is capable of producing and separating electron hole pairs caused by photons absorbed in the depletion region, further comprising the fabrication of a transistor body 8108-8114-8110 at the same time as the fabrication of the silicon of the heterojunction. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

With regard to claims 5-10 Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium 108 on silicon 191 heterojunction stack comprising a silicon layer 191 (6301 in figure 55a) comprising substantially silicon for conducting light, a germanium layer 108 (6302 in figure 55a) com-

prising substantially germanium for conducting light; and a cladding 104-5109 comprised of a plurality of dielectric materials, a first plurality of conductive contacts 120 coupled to said germanium layer 108 (6302 in figure 55a), and a second plurality of conductive contacts 118,122 (800 in fig. 43) coupled to said silicon layer 191, wherein the germanium 108 on silicon 191 heterojunction forms a diode structure with a depletion region, where the diode structure is capable of producing and separating electron hole pairs caused by photons absorbed in the depletion region, wherein the cladding 104-5109 further comprises a bottom cladding 104 comprised of the insulating layer of an SOI 152 that also serves as the substrate of a CMOS integrated circuit 5101, and a top and side cladding 5109, where each of the claddings is comprised of a plurality of dielectric materials, one of the plurality of dielectric materials comprising the top and side cladding 5109 are formed from the same film as an inter-layer dielectric film, gate spacer, dielectric spacer, passivation film, isolation dielectric or field oxide of a floating body or body tied CMOS transistor 8101. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

With regard to claims 12-19 Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium 108 on silicon 191 heterojunction stack comprising a silicon layer 191 (6301 in figure 55a) comprising substantially silicon for conducting light, a germanium layer 108 (6302 in figure 55a) comprising substantially germanium for conducting light; and a cladding 104-5109 com-

prised of a plurality of dielectric materials, a first plurality of conductive contacts 120 coupled to said germanium layer 108 (6302 in figure 55a), and a second plurality of conductive contacts 118,122 (800 in fig. 43) coupled to said silicon layer 191, wherein the germanium 108 on silicon 191 heterojunction forms a diode structure with a depletion region, where the diode structure is capable of producing and separating electron hole pairs caused by photons absorbed in the depletion region, wherein each of the second plurality of conductive contacts 800 comprises a metal silicide ohmic contact to the silicon layer 191 of the heterojunction, and a tungsten conductive plug 5121 with a first terminal coupled to the ohmic contact and a second terminal coupled to a metal layer 5120 of an integrated circuit 5101 (note figures 43-44) and the conductive plug 5121 is formed simultaneously with the metal layer 5120, further comprising the fabrication of an ohmic contact on the source, drain, body, or gate of a transistor 8101 at the same time as the fabrication of an ohmic contact on the silicon of the heterojunction; the fabrication of a conductive plug 5121 to an ohmic contact of a transistor 8101 at the same time as the fabrication of the conductive plug 5121 to an ohmic contact to the silicon of the heterojunction, and the fabrication of a tungsten or aluminum local interconnection between a pair of transistors 8101-9101, at the same time as fabricating a local interconnection for coupling an ohmic contact on the silicon of the heterojunction with an ohmic contact on one of the transistors 8101-9101. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

With regard to claim 20 Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium 108 on silicon 191 heterojunction stack comprising a silicon layer 191 (6301 in figure 55a) comprising substantially silicon for conducting light, a germanium layer 108 (6302 in figure 55a) comprising substantially germanium for conducting light; and a cladding 104-5109 comprised of a plurality of dielectric materials, a first plurality of conductive contacts 120 coupled to said germanium layer 108 (6302 in figure 55a), and a second plurality of conductive contacts 118,122 (800 in fig. 43) coupled to said silicon layer 191, wherein the germanium 108 on silicon 191 heterojunction forms a diode structure with a depletion region, where the diode structure is capable of producing and separating electron hole pairs caused by photons absorbed in the depletion region, wherein at least one contact of the pluralities of contacts is coupled to a metal layer 5120 on an integrated circuit 5101 (note figures 43-44), where the metal layer 5120 has a coupling to a resistor, inductor, capacitor, diode, bond pad, or transistor 8101 on the integrated circuit 5101. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

With regard to claim 21 Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium 108 on silicon 191 heterojunction stack comprising a silicon layer 191 (6301 in figure 55a) comprising substantially silicon for conducting light, a germanium layer 108 (6302 in figure 55a) com-

prising substantially germanium for conducting light; and a cladding 104-5109 comprised of a plurality of dielectric materials, a first plurality of conductive contacts 120 coupled to said germanium layer 108 (6302 in figure 55a), and a second plurality of conductive contacts 118,122 (800 in fig. 43) coupled to said silicon layer 191, wherein the germanium 108 on silicon 191 heterojunction forms a diode structure with a depletion region, where the diode structure is capable of producing and separating electron hole pairs caused by photons absorbed in the depletion region, wherein each of the first plurality of conductive contacts 120 comprises an ohmic contact to the germanium of the heterojunction, and a conductive plug 5121 with a first terminal coupled to the ohmic contact and a second terminal coupled to a metal layer 5120 of an integrated circuit 5101 (note figures 43-44). Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

With regard to claims 22-27 Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium 108 on silicon 191 heterojunction stack comprising a silicon layer 191 (6301 in figure 55a) comprising substantially silicon for conducting light, a germanium layer 108 (6302 in figure 55a) comprising substantially germanium for conducting light; and a cladding 104-5109 comprised of a plurality of dielectric materials, a first plurality of conductive contacts 120 coupled to said germanium layer 108 (6302 in figure 55a), and a second plurality of conductive contacts 118,122 (800 in fig. 43) coupled to said silicon layer 191, wherein

the germanium 108 on silicon 191 heterojunction forms a diode structure with a depletion region, where the diode structure is capable of producing and separating electron hole pairs caused by photons absorbed in the depletion region, further comprising the introduction of a first plurality of dopants into a plurality of regions in the silicon layer 191 of the heterojunction and the silicon body of a transistor 8101, and the introduction of a second plurality of dopants into a plurality of regions in the germanium layer 108 (6302 in figure 55a) of the heterojunction, wherein the first plurality of dopants is comprised of dopants with electrical charge opposite or equal to the polarity of the dopants comprising the second plurality of dopants. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

With regard to claims 28-33 Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium 108 on silicon 191 heterojunction stack comprising a silicon layer 191 (6301 in figure 55a) comprising substantially silicon for conducting light, a germanium layer 108 (6302 in figure 55a) comprising substantially germanium for conducting light; and a cladding 104-5109 comprised of a plurality of dielectric materials, a first plurality of conductive contacts 120 coupled to said germanium layer 108 (6302 in figure 55a), and a second plurality of conductive contacts 118,122 (800 in fig. 43) coupled to said silicon layer 191, wherein the germanium 108 on silicon 191 heterojunction forms a diode structure with a depletion region, where the diode structure is capable of producing and separating electron

hole pairs caused by photons absorbed in the depletion region, further comprising a silicon waveguide 160 with an input and an output; and, a transistor 8101 with polysilicon gate; a polysilicon optical structure mode converter 5110 with an input and an output, where the output of the mode converter 5110 is coupled to the input of the waveguide photodetector, and the input to the mode converter 5110 is coupled to the output of the silicon waveguide 160, wherein the mode converter 5110 is comprised of a plurality of dielectric structures introduced in substantial proximity to the input to the waveguide photodetector. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

With regard to claim 38 A semiconductor chip comprising a germanium on silicon waveguide photodetector located on the semiconductor chip, said germanium on silicon waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium 108 on silicon 191 heterojunction stack comprising a silicon layer 191 (6301 in figure 55a) comprising substantially silicon for conducting light, and a germanium layer 108 (6302 in figure 55a) comprising substantially germanium for conducting light; and a cladding 104-5109 comprised of a plurality of dielectric materials; an optical input; a first plurality of conductive contacts 120 coupled to said germanium layer 108 (6302 in figure 55a); and a second plurality of conductive contacts 118,122 (800 in fig. 43) coupled to said silicon layer 191; and, inputs for receiving optical signals; outputs for outputting electrical signals; and, a semiconductor device 5101 connected to

the germanium on silicon waveguide photodetector outputs and located on the semi-conductor chip. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

With regard to claim 44 Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium 108 on silicon 191 heterojunction, and cladding 104-5109 comprised of a plurality of dielectric materials, a first plurality of conductive contacts 120 coupled to the germanium 108 and not coupled to the silicon 191; a second plurality of conductive contacts 118,122 (800 in fig. 43) coupled to the silicon 191 and not coupled to the germanium 108, and wherein said first plurality of conductive contacts 120 are displaced from said second plurality of conductive contacts 118,122; and, a transistor body 8108-8114-8110 fabricated at the same time as the fabrication of the silicon of the heterojunction. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

With regard to claim 45 Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium 108 on silicon 191 heterojunction wherein the germanium 108 on silicon 191 heterojunction forms a diode structure with a depletion region, where the diode structure is capable of producing and separating electron hole pairs caused by photons absorbed in the depletion region, and a cladding 104-5109 comprised of a plurality of dielectric materials; and, a first plurality of conductive contacts 120 coupled to the germanium 108; and, a second plurality of

conductive contacts 118,122 (800 in fig. 43) coupled to the silicon 191. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

With regard to claims 46-50 Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium 108 on silicon 191 heterojunction, a cladding 104-5109 comprised of a plurality of dielectric materials; a first plurality of conductive contacts 120 coupled to the germanium 108, and a second plurality of conductive contacts 118,122 (800 in fig. 43) coupled to the silicon 191; wherein the cladding 104-5109 comprises a bottom cladding 104 comprised of the insulating layer of an SOI 152 that also serves as the substrate of a CMOS integrated circuit 5101, and a top and side cladding 5109, where each of the claddings is comprised of a plurality of dielectric materials, and one of the plurality of dielectric materials comprising the top and side cladding 5109 is formed from the same film as a dielectric component of a transistor 8101, where the dielectric component is selected from a group comprising an inter-layer dielectric film, a gate spacer, a silicide block, a dielectric spacer, a passivation film, an isolation dielectric and a field oxide. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

With regard to claims 51-58 Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium 108 on silicon 191 heterojunction, and a cladding 104-5109 comprised of a plurality of dielectric materials, a first plurality of conductive contacts 120 coupled to the germanium 108, and a

second plurality of conductive contacts 118,122 (800 in fig. 43) coupled to the silicon 191 wherein each of the second plurality of conductive contacts 800 comprises a metal silicide ohmic contact to the silicon of the heterojunction, and a tungsten conductive plug 5121 with a first terminal coupled to the ohmic contact and a second terminal coupled to a metal layer 5120 of an integrated circuit 5101 (note figures 43-44), wherein the conductive plug 5121 is formed simultaneously with the metal layer 5120, and further comprising the fabrication of an ohmic contact on the source, drain, body, or gate of a transistor 8101 at the same time as the fabrication of an ohmic contact on the silicon of the heterojunction, the fabrication of a conductive plug 5121 to an ohmic contact of a transistor 8101 at the same time as the fabrication of a conductive plug 5121 to an ohmic contact to the silicon of the heterojunction, and the fabrication of a tungsten or aluminum local interconnection between a pair of transistors 8101-9101, at the same time as fabricating a local interconnection for coupling an ohmic contact on the silicon of the heterojunction with an ohmic contact on one of the transistors 8101-9101. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

With regard to claim 59 Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium 108 on silicon 191 heterojunction, and a cladding 104-5109 comprised of a plurality of dielectric materials, a first plurality of conductive contacts 120 coupled to the germanium 108 and not coupled to the silicon 191, and, a second plurality of conductive contacts 118,122 (800 in

fig. 43) coupled to the silicon 191 and not coupled to the germanium 108, wherein said first plurality of conductive contacts 120 are displaced from said second plurality of conductive contacts 118,122; wherein at least one contact of the pluralities of contacts is coupled to a metal layer 5120 on an integrated circuit 5101 (note figures 43-44), where the metal layer 5120 has a coupling to a resistor, inductor, capacitor, diode, bond pad, or transistor 8101 on the integrated circuit 5101. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

With regard to claim 60 Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium 108 on silicon 191 heterojunction, a cladding 104-5109 comprised of a plurality of dielectric materials, a first plurality of conductive contacts 120 coupled to the germanium 108 wherein each of the first plurality of conductive contacts 120 comprises an ohmic contact to the germanium of the heterojunction, and a conductive plug 5121 with a first terminal coupled to the ohmic contact and a second terminal coupled to a metal layer 5120 of an integrated circuit 5101 (note figures 43-44), and; a second plurality of conductive contacts 118,122 (800 in fig. 43) coupled to the silicon 191. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

With regard to claims 61,63, and 64 Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium 108 on silicon 191 heterojunction, a cladding 104-5109 comprised of a plurality of dielectric ma-

terials; a first plurality of conductive contacts 120 coupled to the germanium 108 and not coupled to the silicon 191; and a second plurality of conductive contacts 118,122 (800 in fig. 43) coupled to the silicon 191 and not coupled to the germanium 108, wherein said first plurality of conductive contacts 120 are displaced from said second plurality of conductive contacts 118,122, wherein a plurality of regions in the silicon 191 of the heterojunction comprise a first plurality of dopants introduced at the same time as the introduction of a plurality of dopants into a plurality of regions in the silicon body of a transistor 8101(claim 61), a plurality of regions in the germanium 108 of the heterojunction comprise a second plurality of dopants, and the first plurality of dopants is comprised of dopants with electrical charge opposite (claim 63) or equal (claim 64) to the polarity of the dopants comprising the second plurality of dopants. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

With regard to claims 65-67 Delwala discloses a waveguide photodetector having an input and comprising a silicon waveguide 160 with an input and an output and comprising a core 190 comprised of a germanium 108 on silicon 191 heterojunction, a cladding 104-5109 comprised of a plurality of dielectric materials, a first plurality of conductive contacts 120 coupled to the germanium 108; a second plurality of conductive contacts 118,122 (800 in fig. 43) coupled to the silicon 191; a transistor 8101 having a polysilicon gate; and a polysilicon optical structure mode converter 5110 with an input and an output, where the output of the mode converter 5110 is coupled to the input of the

waveguide photodetector, and where the input to the mode converter 5110 is coupled to the output of the silicon waveguide 160 and the mode converter 5110 is comprised of a plurality of dielectric structures introduced in substantial proximity to the input to the waveguide photodetector. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

With regard to claim 71 Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium 108 on silicon 191 heterojunction, and cladding 104-5109 comprised of a plurality of dielectric materials, a first plurality of electrical contacts 120 coupled to the germanium 108; a second plurality of electrical contacts 118,122 (800 in fig. 43) coupled to the silicon 191; and, a transistor body 8108-8114-8110 fabricated at the same time as the fabrication of the silicon of the heterojunction and wherein the transistor body 8108-8114-8110 is external to the waveguide 160 and displaced from the waveguide 160. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

With regard to claim 72 Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium 108 on silicon 191 heterojunction, and a cladding 104-5109 comprised of a plurality of dielectric materials, a first plurality of conductive contacts 120 coupled to the germanium 108, and a second plurality of conductive contacts 118,122 (800 in fig. 43) coupled to the silicon 191, wherein at least one contact of the pluralities of contacts is electrically coupled to a

metal layer 5120 on an integrated circuit 5101 (note figures 43-44), where the metal layer 5120 has a an electrical to a resistor, inductor, capacitor, diode, bond pad, or transistor 8101 on the integrated circuit 5101 external to the waveguide 160 and displaced from the waveguide 160. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

With regard to claim 73 Delwala discloses a waveguide photodetector comprising a waveguide 160 comprising a core 190 comprised of a germanium 108 on silicon 191 heterojunction wherein a plurality of regions in the silicon of the heterojunction comprise a plurality of dopants introduced at the same time as the introduction of a plurality of dopants into a plurality of regions in the silicon body of a transistor 8101 and wherein the transistor 8101 is external to the waveguide 160 and displaced from the waveguide 160, and a cladding 104-5109 comprised of a plurality of dielectric materials; a first plurality of electrical contacts 120 coupled to the germanium 108; and a second plurality of electrical contacts 118,122 (800 in fig. 43) coupled to the silicon 191. Note figures 1-10, 13-18, 43-54, and paragraphs 0084-0132 and 0245-0266 of Delwala.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Sue A. Purvis, at 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thomas L. Dickey/
Primary Examiner
Art Unit 2826